UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,438	11/12/2003	Torsten Partsch	2003P52601US/I331.102.101	7153

7590 07/09/2008

Dicke, Billig & Czaja, PLLC
Fifth Street Towers
Suite 2250
100 South Fifth Street
Minneapolis, MN 55402

EXAMINER	
PATEL, KAUSHIKKUMAR M	
ART UNIT	PAPER NUMBER
2188	

MAIL DATE	DELIVERY MODE
07/09/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/706,438	PARTSCH, TORSTEN	
	Examiner	Art Unit	
	KAUSHIKKUMAR PATEL	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Reopening of Prosecution after Appeal

1. In view of the appeal brief filed on April 11, 2008, PROSECUTION IS HEREBY REOPENED. New grounds of rejections are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Hyung S Sough/
Supervisory Patent Examiner, Art Unit 2188

Claim Objections

2. Claim 35 is objected to because of the following informalities:

Claim 35 recites the limitation “bypassing first in first out memory cells used to provide data if the column address strobe latency is greater than one”. The examiner

believes the limitation should be -- if the column address strobe latency is one-- and treated accordingly during this office action.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 31, 34 and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe (US 2001/0017790).

As per claim 1, Watanabe teaches a random access memory (par. [0002]), comprising:

an array of memory cells (par. [0003], see claim 1);

a memory configured to receive data from the array of memory cells (fig. 4, item 35);

a bypass circuit configured to receive the data from the array of memory cells and to bypass the memory (fig. 4, item P1; par. [0038]); and

a circuit (fig. 4, items 36, 37) configured to select between receiving the data from the memory to provide first output signals (fig. 4, S2) and receiving the data from the bypass circuit to provide second output signals (fig. 4, S1) based on a column

address strobe latency select signal (pars. [0017], [0041]).

As per claim 2, Watanabe teaches, wherein the circuit is configured to receive the data from the bypass circuit and provide the second output signals if the column address strobe latency select signal indicates a column address strobe latency value of one (par. [0044]).

As per claim 3, Watanabe teaches, wherein the circuit is configured to receive the data from the memory and provide the first output signals if the column address strobe latency select signal indicates a column address strobe latency value of greater than one (par. [0044]).

As per claim 31, Watanabe teaches a random access memory (par. [0002[, claim 1) comprising:

means for storing data read from an array of memory cells (fig. 4, item 35);

means for receiving the data read from the array of memory cells to bypass the means for storing data (fig. 4, item P1, par. [0038];

means for retrieving the data from the means for storing the data if column address strobe latency is greater than one (par. [0044]);

means for retrieving the data from the means for receiving the data if the column address strobe latency is one (par. [0044]).

As per claim 34, Watanabe teaches a method for reading data from a random access memory in a column address strobe latency of one (par. [0011), comprising:

initiating a read command on a first edge of a clock cycle (pars. [0011], [0064]);

receiving data read from the array of memory cells in a bypass circuit during the clock cycle (pars. [0011], [0064]); and

retrieving the data from the bypass circuit during the clock cycle (pars. [0011], [0064]).

As per claim 35, Watanabe teaches the method of claim 34, comprising bypassing first in/first out memory cells used to provide data if the column address strobe latency is one (see objection to the claim above) (par. [0044]).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 12-18, 24 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (US 2001/0017790).

As per claim 12, Watanabe teaches bypass circuit with output (fig. 4, S1) with two states (e.g. 0 and 1), but fails to teach tri-state output as required by the claim. However, the use of tri-state output is well known in the art and the examiner takes

official notice of the fact. Thus, it would have been obvious to one having ordinary skill in the art at the time of the invention to use tri-state output, because tri-state output provides three states (e.g. low (0), high (1) and Hi-Z (or off)), wherein the third state (Hi-Z) isolates (turns off) the floating output from the circuit, which allows multiple circuits to use same output (e.g. when CAS latency is greater than one, the Hi-Z state isolates the output from bypass circuit, allowing output from FIFO circuit to pass data).

As per claim 13, Watanabe teaches a memory (e.g. register block) for storing data received from an array of memory cells (see claim 1 above). Watanabe fails to teach memory is a first in first out memory (FIFO), however the use of FIFO for storing data is well known in the art and the examiner takes official notice of the fact. Thus, it would have been obvious to one having ordinary skill in the art at the time of the invention to utilize FIFO memory instead of register blocks in the system of Watanabe because FIFO storage allows easier flow control and maintains the program order to avoid any false data access.

As to claims 14, 15 and 16, Watanabe teaches synchronous random access memory (SDRAM) (par. [0002]), but fails to teach low power SDRAM, a double data rate-I (DDR) SDRAM and DDR-II SDRAM. However, the technology of a low power SDRAM as well as DDR-I and DDR-II SDRAM is well known in the art (see applicant's disclosure, page 1, lines 7-29) and the examiner takes official notice of the fact. Thus, it would have been obvious to use a low power SDRAM, DDR-I SDRAM and DDR-II

SDRAM in the system of Watanabe to reduce the power consumption and/or increase the data retrieval speed.

As per claim 17, Watanabe teaches a random access memory (par. [0002], comprising:

a memory (fig. 4, item 35);

a bypass circuit that bypasses the memory (fig. 4, item P1, par. [0038]); and

a control circuit (fig. 4, item 37) configured to provide first signals (fig. 4, item S2) and second signals (fig. 4, item S1), wherein the first signals latch data from the memory to provide a column address strobe latency of greater than one and the second signals latch data from the bypass circuit to provide a column address strobe latency of one (pars. [0017], [0044]).

Watanabe teaches the memory is a register block (fig. 4, item 35), but fails to teach first in first out memory (FIFO). The use of FIFO for storing data is well known in the art and the examiner takes official notice of the fact. Thus, it would have been obvious to one having ordinary skill in the art at the time of the invention to utilize FIFO memory instead of register blocks in the system of Watanabe because FIFO storage allows easier flow control and maintains the program order to avoid any false data access.

As per claim 18, Watanabe teaches, wherein the control circuit comprises a clock signal multiplexer configured to select between providing the first signals and the

second signals based on a column address strobe latency select signal (fig. 4, items 36 and 37, pars. [0038], [0041], [0044], the control circuit and switching circuit selects between S1 and S2 based on CAS latency value, which means control and switching circuits can be considered as clock signal multiplexer).

Claim 24 is rejected under same rationales as applied to claim 12 above.

Claim 32 is rejected under same rationales as applied to claim 13 above.

7. Claims 4-11, 19-23, 33 and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (US 2001/0017790) as applied to claims 1, 17, 31 and 34 above, and further in view of Edo (US 6,282,150) and/or Hamamoto et al. (US 6,417,715) and/or Matsudera et al. (US 6,801,144).

As per claims 4 and 6, Watanabe teaches all the limitations of claim 1, but fails to teach first and second rise and fall circuits respectively for the memory and bypass circuits. Edo teaches a semiconductor memory outputting data synchronously with the rise and fall phases of the reference clock one bit at a time (Edo, abstract, col. 1, lines 6-32). Hamamoto teaches semiconductor memory device using clock generation circuit that generates internal clocks based on external reference clocks to serialize data output with rising and falling edges of the clock (Hamamoto, abstract, col. 1, lines 10-32; col. 2, lines 9-25). Matsudera teaches rise and fall circuits for serializing input/output bits to/from memory cells (Matsudera, abstract, col. 7, lines 36-61). It would have been obvious to one having ordinary skill in the art at the time of the invention to use rise and

fall circuits (first and second, each for FIFO memory and bypass circuit) as taught by Edo, Hamamoto and Matsudera in the system of Watanabe to serialize and/or synchronize data access to improve the performance of the memory.

As per claims 5 and 7, Watanabe, Edo, Hamamoto and Matsudera teach wherein the circuit is configured to provide the first rise and fall signals after a first clock cycle is completed following a read command that is initiated by a first edge of the first clock cycle (Watanabe teaches providing signal after the read command is issued, pars. [0011], [0064]. As explained above (claims 4 and 6), the rise and fall signals are also applied to serialize and/or synchronize data access one bit at a time).

As per claim 8, Watanabe teaches wherein the circuit comprises a multiplexer configured to select between serialized data from the first circuit and serialized data from the second circuit based on the column address strobe latency select signal (fig. 4, items 36 and 37, pars. [0038], [0041], [0044], the control circuit and switching circuit selects between S1 and S2 based on CAS latency value, which means control and switching circuits can be considered as clock signal multiplexer).

Claims 9 and 10 rejected under same rationales as applied to claims 4-7 above.

As per claim 11, the sequence of applying various signals is inherent in the combined system of Watanabe, Edo, Hamamoto and Matsudera, otherwise the system

will provide wrong data and it will fail because without proper synchronization of all the signals the data output will be erroneous.

Claim 19 is rejected under same rationales as applied to claims 4 and 6 above.

As per claim 20, Hamamoto and Edo teach wherein the control circuit is configured to provide the first signals comprising a first rise signal and a first fall signal that is the inverse of the first rise signal and the second signals comprising a second rise signal and a second fall signal that is the inverse of the second rise signal (Hamamoto, col. 4, lines 15-18; Edo, col. 17, lines 18-45).

As per claim 21, Edo teaches wherein the rise/fall circuit is configured to provide a first data bit as output on a rising edge of the first rise signal and a second data bit as output on arising edge of the first fall signal (Edo, col. 18, lines 15-18).

As per claim 22, Hamamoto teaches comprising a data delay circuit electrically coupled to the rise/fall .circuit and configured to adjust output timing of the data (Hamamoto, fig. 2, items 130 and 150).

As per claim 23, Watanabe, Edo, Hamamoto and Matsudera explicitly fail to teach driver to pass data from the delay circuit to a data pad, however the driver is inherent in the system to provide data at output data pad.

Claim 33 is rejected under same rationales as applied to claims 4 and 6.

Claims 36-38 are rejected under the same rationales as applied to claims 20-23.

8. Claims 25-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (US 2001/0017790) and further in view of Edo (US 6,282,150) and/or Hamamoto et al. (US 6,417,715) and/or Matsudera et al. (US 6,801,144).

As per claim 25, Watanabe teaches a random access memory, comprising:

a memory circuit (fig. 4, item 35);

a bypass circuit configured to bypass the memory circuit (fig. 4, item P1, par. [0038]).

Watanabe further teaches a first output signal (fig. 4, item S2) and a second output signal (fig. 4, item S1) and a multiplexer configured to select between the first output signal and the second output signal based on a column address strobe latency select signal (fig. 4, items 36 and 37, pars. [0017], [0038], [0044]).

Watanabe fails to teach a first rise/fall circuit configured to receive data from the memory circuit and a second rise/fall circuit configured to receive data from the bypass circuit. Edo teaches a semiconductor memory outputting data synchronously with the rise and fall phases of the reference clock one bit at a time (Edo, abstract, col. 1, lines 6-32). Hamamoto teaches semiconductor memory device using clock generation circuit that generates internal clocks based on external reference clocks to serialize data output with rising and falling edges of the clock (Hamamoto, abstract, col. 1, lines 10-32;

col. 2, lines 9-25). Matsudera teaches rise and fall circuits for serializing input/output bits to/from memory cells (Matsudera, abstract, col. 7, lines 36-61). It would have been obvious to one having ordinary skill in the art at the time of the invention to use rise and fall circuits (first and second, each for FIFO memory and bypass circuit) as taught by Edo, Hamamoto and Matsudera in the system of Watanabe to serialize and/or synchronize data access to improve the performance of the memory.

Claims 26-30 are also rejected under same rationales as applied to claims 4-8 and 19-23 above.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAUSHIKKUMAR PATEL whose telephone number is (571)272-5536. The examiner can normally be reached on 7.30 am - 4.00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hyung S Sough/
Supervisory Patent Examiner, Art Unit 2188
07/07/08

KAUSHIKKUMAR PATEL
Examiner
Art Unit 2188

/kmp/